ST2329B

2-bit dual supply level translator without direction control pin, open drain output

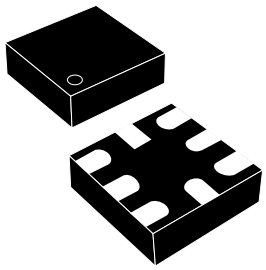
Datasheet —preliminary data

Features

- 18 Mbps (max.) data rate when driven by a totem pole driver
- 6.8 Mbps (max.) data rate when driven by an open drain pole driver
- Bi-directional level translation without direction control pin
- Wide V_L voltage range of 1.65 to 3.6 V
- Wide V_{CC} voltage range of V_L to 5.5 V
- Power-down mode feature: when either supply is OFF, all I/Os are in high impedance
- Low quiescent current (max. 4 µA)
- Able to be driven by totem pole and open drain drivers
- 5.5 V tolerant Enable pin
- ESD performance on all pins: ±2 kV HBM
- Small package and footprint: QFN8 (1.4 x 1.2 x 0.55 mm) package

Applications

- Low-voltage system level translation
- Mobile phones and other mobile devices
- I^2C level translation
- UART level translation



QFN8
(1.4 x 1.2 x 0.55 mm)

Table 1. Device summary

Order code	Package	Packing	Package topmark
ST2329BQTR	QFN8 (1.4 x 1.2 x 0.55 mm)	Tape and reel (3000 parts per reel)	3A

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Description

The ST2329B is a 2-bit dual supply level translator which provides the level shifting capability to allow data transfer in a multi-voltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. It utilizes a transmission gate-based design that allows bi-directional level translation without a control pin.

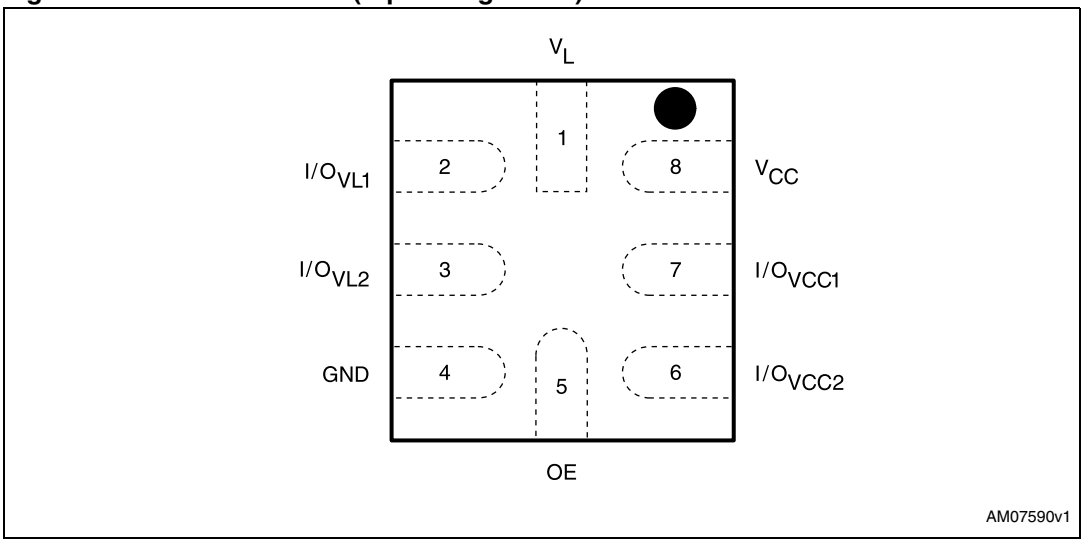
The ST2329B accepts V_L from 1.65 to 3.6 V and V_{CC} from 1.80 to 5.5 V, making it ideal for data transfer between low-voltage ASICs/PLD and higher voltage systems. This device has a tri-state output mode which can be used to disable all I/Os.

The ST2329B supports power-down mode when V_{CC} is grounded/floating and the device is disabled via the OE pin.

2 Pin settings

2.1 Pin connection

Figure 1. Pin connection (top through view)



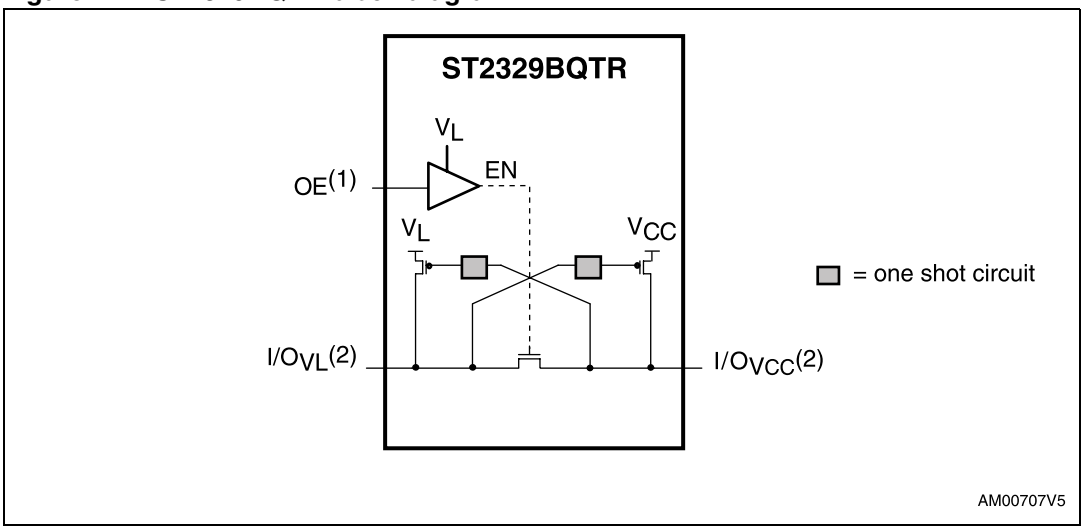
2.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	V_L	Supply voltage
2	I/O_{VL1}	Data input/output
3	I/O_{VL2}	Data input/output
4	GND	Ground
5	OE	Output enable
6	I/O_{VCC2}	Data input/output
7	I/O_{VCC1}	Data input/output
8	V_{CC}	Supply voltage

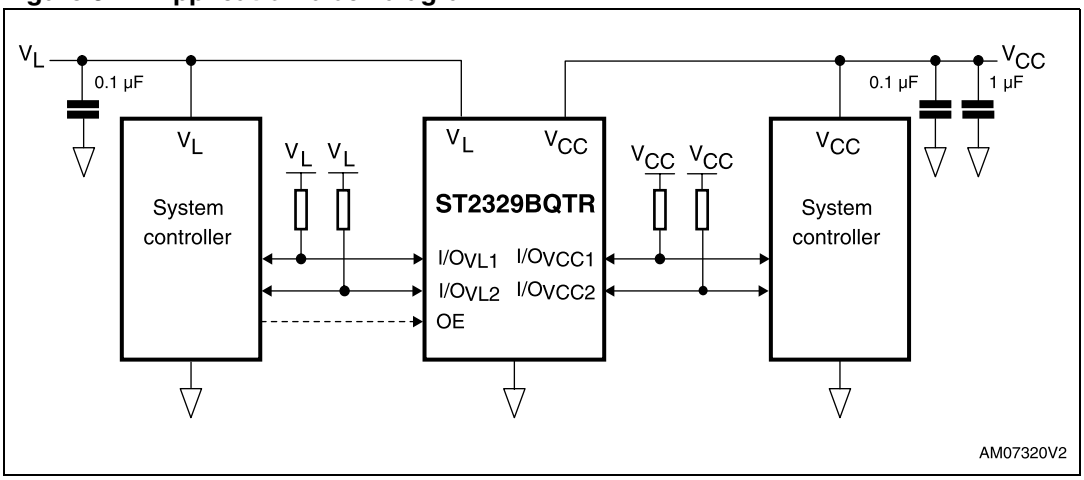
3 Device block diagrams

Figure 2. ST2329BQTR block diagram



1. When OE is LOW, all I/Os are in high-impedance mode.
2. The ST2329BQTR has 2 channels. For simplicity, the diagram above shows only 1 channel.

Figure 3. Application block diagram



4 Supplementary notes

4.1 Driver requirements

The ST2329BQTR may be driven by an open drain or totem pole driver and the nature of the device output is “open drain”. It must not be used to drive a pull-down resistor as the impedance of the output at HIGH state depends on the pull-up resistor placed at the I/Os.

As the device has pull-up resistors on both the I/O_{VCC} and I/O_{VL} ports, the user needs to ensure that the driver is able to sink the required amount of current. For example, if the settings are V_{CC} = 5.5 V, V_L = 4.3 V, and the pull-up resistor is 10 kΩ, then the driver must be able to sink at least (5.5 V / 10 kΩ) + (4.3 V / 10 kΩ) = 1 mA and still meet the V_{IL} requirements of the ST2329BQTR.

4.2 Load driving capability

To support the open drain system, the one-shot transistor is turned on only during high transition at the output side. When it drives a high state, after the one-shot transistor is turned off, only the pull-up resistor is able to maintain the state. In this case, the resistive load is not recommended.

4.3 Power-off feature

In some applications where it may be required to turn off one of the power supplies powering up the level translator, the user can turn off the V_{CC} only when the OE pin is low (device is disabled). There is no current consumption in V_L due to floating gates or other causes, and the I/Os are in a high-impedance state in this mode.

4.4 Truth table

Table 3. Truth table

Enable	Bi-directional input/output	
OE	**I/O_{VCC}**	**I/O_{VL}**
H(1)	H(2)	H(1)
H(1)	L	L
L	Z(3)	Z(3)

1. High level V_L power supply referred.
2. High level V_{CC} power supply referred.
3. Z = high-impedance.

5 Maximum rating

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_L	Supply voltage	-0.3 to 4.6	V
V_{CC}	Supply voltage	-0.3 to 6.5	V
V_{OE}	DC control input voltage	-0.3 to 6.5	V
$V_{I/OVL}$	DC I/O_{VL} input voltage (OE = GND or V_L)	-0.3 to V_L + 0.3	V
$V_{I/OVCC}$	DC I/O_{VCC} input voltage (OE = GND or V_L)	-0.3 to V_{CC} + 0.3	V
I_{IK}	DC input diode current	-20	mA
$I_{I/OVL}$	DC output current	±25	mA
$I_{I/OVCC}$	DC output current	±25	mA
I_{SCTOUT}	Short-circuit duration, continuous	40	mA
P_D	Power dissipation(1)	500	mW
T_{STG}	Storage temperature	-65 to 150	°C
TL	Lead temperature (10 seconds)	300	°C
ESD	Electrostatic discharge protection (HBM)	±2	kV

1. 500 mW: 65 °C derated to 300 mW by 10 mW / °C: 65 °C to 85 °C.

Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_L	Supply voltage	1.65	–	3.6	V
V_{CC}	Supply voltage	V_L	–	5.5	V
V_{OE}	Input voltage (OE output enable pin, V_L power supply referred)	0	–	3.6	V
$V_{I/OVL}$	I/O_{VL} voltage	0	–	V_L	V
$V_{I/OVCC}$	I/O_{VCC} voltage	0	–	V_{CC}	V
T_{op}	Operating temperature	-40	–	85	°C
dt/dV	Input rise and fall time	0	–	1	ns/V

6 Electrical characteristics

6.1 DC characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25 °C.

Table 6. DC characteristics

Symbol	Parameter	V_L	V_{CC}	Test conditions	Value					Unit
					T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IHL}	High level input voltage (I/O_{VL})	1.65	V_L to 5.5	–	1.4	–	–	1.4	–	V
		2.0			1.6	–	–	1.6	–	
		2.5			2.0	–	–	2.0	–	
		3.0			2.4	–	–	2.4	–	
		3.6			2.8	–	–	2.8	–	
V_{ILL}	Low level input voltage (I/O_{VL})	1.65	V_L to 5.5	–	–	–	0.3	–	0.3	V
		2.0			–	–	0.4	–	0.4	
		2.5			–	–	0.5	–	0.5	
		3.0			–	–	0.6	–	0.6	
		3.6			–	–	0.8	–	0.8	
V_{IHC}	High level input voltage (I/O_{VCC})	1.65 to V_{CC}	1.8	–	1.6	–	–	1.6	–	V
			2.5		2.3	–	–	2.3	–	
			3.0		2.7	–	–	2.7	–	
			3.6		3.3	–	–	3.3	–	
			4.3		3.5	–	–	3.5	–	
			5.5		4.2	–	–	4.2	–	
V_{ILC}	Low level input voltage (I/O_{VCC})	1.65 - 2.5	3 - 5.5	–	–	–	–	0.3	–	V
		2.7 - 3.6	3.6 - 5.5	–	–	–	–	0.5	–	
V_{IH-OE}	High level input voltage (OE)	1.65	V_L to 5.5	–	1.0	–	–	1.0	–	V
		2.0			1.2	–	–	1.2	–	
		2.5			1.4	–	–	1.4	–	
		3.0			1.6	–	–	1.6	–	
		3.6			2.0	–	–	2.0	–	

Table 6. DC characteristics (continued)

Symbol	Parameter	V_L	V_{CC}	Test conditions	Value					Unit
					T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IL-OE}	Low level input voltage (OE)	1.65	V_L to 5.5		–	–	0.33	–	0.33	V
		2.0			–	–	0.40	–	0.40	
		2.5			–	–	0.50	–	0.50	
		3.0			–	–	0.60	–	0.60	
		3.6			–	–	0.75	–	0.75	
V_{OLL}	Low level output voltage (I/O_{VL})	1.65 to 3.6	V_L to 5.5	IO = 1.0 mA $I/O_{VCC} \leq 0.15$ V	–	–	0.40	–	0.40	V
V_{OLC}	Low level output voltage (I/O_{VCC})	1.65 to 3.6	V_L to 5.5	IO = 1.0 mA $I/O_{VL} \leq 0.15$ V	–	–	0.40	–	0.40	V
I_{OE}	Control input leakage current (OE)	1.65 to 3.6	V_L to 5.5	V_{OE} = GND or V_L	–	–	±0.1	–	±0.1	µA
I_{IO_LKG}	High impedance leakage current (I/O_{VL}, I/O_{VCC})	1.65 to 3.6	V_L to 5.5	OE = GND	–	–	±0.1	–	±0.1	µA
I_{QVCC}	Quiescent supply current V_{CC}	1.65 to 3.6	V_L to 5.5	Only pull-up resistor connected to I/O	–	3	3.5	–	4	µA
I_{QVL}	Quiescent supply current V_L	1.65 to 3.6	V_L to 5.5	only pull-up resistor connected to I/O	–	0.01	0.1	–	1	µA
I_{Z-VCC}	High impedance quiescent supply current V_{CC}	1.65 to 3.6	V_L to 5.5	OE = GND; only pull-up resistor connected to I/O	–	3	3.5	–	4	µA
I_{Z-VL}	High impedance quiescent supply current V_L	1.65 to 3.6	V_L to 5.5	OE = GND; only pull-up resistor connected to I/O	–	0.01	0.1	–	1	µA

6.2 AC characteristics

6.2.1 Device driven by open drain driver

Load C_L = 15 pF; R_{up} = 4.7 kΩ; driver $t_r = t_f \leq 6$ ns over temperature range -40 °C to 85 °C.

Table 7. AC characteristics - test conditions: V_L = 1.65 - 1.8 V (device driven by open drain driver)

Symbol	Parameter		V_{CC} = 1.8 - 2.5 V		V_{CC} = 2.7 - 3.6 V		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}		–	80.0	–	60.0	–	45.0	ns
t_{FVCC}	Fall time I/O_{VCC}		–	23.2	–	33.9	–	53.3	ns
t_{RVL}	Rise time I/O_{VL}		–	60.0	–	45.0	–	35.0	ns
t_{FVL}	Fall time I/O_{VL}		–	16.4	–	17.6	–	16.9	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	–	3.4	–	2.0	–	2.0	ns
		t_{PHL}	–	13.9	–	19.1	–	30.2	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-LH}	t_{PLH}	–	2.0	–	2.0	–	2.6	ns
		t_{PHL}	–	8.6	–	9.0	–	9.5	ns
t_{PZL} t_{PLZ}	Output enable and disable time	En	–	10	–	10	–	10	ns
		Dis	–	40	–	40	–	40	ns
D_R	Data rate(1)		–	1.8	–	2.2	–	3.4	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Table 8. AC characteristics - test conditions: V_L = 2.5 - 2.7 V (device driven by open drain driver)

Symbol	Parameter		V_{CC} = 2.7 - 3.6 V		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}		–	70.0	–	50.0	ns
t_{FVCC}	Fall time I/O_{VCC}		–	14.8	–	19.1	ns
t_{RVL}	Rise time I/O_{VL}		–	50.0	–	35.0	ns
t_{FVL}	Fall time I/O_{VL}		–	9.8	–	10.0	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	–	2.0	–	2.0	ns
		t_{PHL}	–	8.2	–	11.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-LH}	t_{PLH}	–	2.0	–	2.0	ns
		t_{PHL}	–	5.3	–	5.9	ns

Table 8. AC characteristics - test conditions: V_L = 2.5 - 2.7 V (device driven by open drain driver) (continued)

Symbol	Parameter		V_{CC} = 2.7 - 3.6 V		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	
t_{PZL} t_{PLZ}	Output enable and disable time	En	–	6	–	6	ns
		Dis	–	40	–	40	ns
D_R	Data rate(1)		–	2.2	–	3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Table 9. AC characteristics - test conditions: V_L = 2.7 - 3.6 V (device driven by open drain driver)

Symbol	Parameter		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}		–	55.0	ns
t_{FVCC}	Fall time I/O_{VCC}		–	17.2	ns
t_{RVL}	Rise time I/O_{VL}		–	40.0	ns
t_{FVL}	Fall time I/O_{VL}		–	9.7	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	–	2.0	ns
		t_{PHL}	–	10.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	–	2.0	ns
		t_{PHL}	–	4.8	ns
t_{PZL} t_{PLZ}	Output enable and disable time	En	–	6	ns
		Dis	–	40	ns
D_R	Data rate(1)	–	–	3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

6.2.2 Device driven by totem pole driver

Load C_L = 15 pF; R_{up} = 10 kΩ; driver $t_r = t_f \leq 6$ ns over temperature range -40 °C to 85 °C.

Table 10. AC characteristics - test conditions: V_L = 1.65 - 1.8 V (device driven by totem pole driver)

Symbol	Parameter		V_{CCB} = 1.8 - 2.5 V		V_{CCB} = 2.7 - 3.6 V		V_{CCB} = 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}		–	7.2	–	4.6	–	1.4	ns
t_{FVCC}	Fall time I/O_{VCC}		–	23.2	–	33.9	–	53.3	ns
t_{RVL}	Rise time I/O_{VL}		–	5.9	–	5.7	–	5.5	ns
t_{FVL}	Fall time I/O_{VL}		–	16.4	–	17.6	–	16.9	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	–	5.5	–	4.1	–	3.6	ns
		t_{PHL}	–	13.9	–	19.1	–	30.2	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	–	4.5	–	3.9	–	3.6	ns
		t_{PHL}	–	8.6	–	9.0	–	9.5	ns
t_{PZL} t_{PLZ}	Output enable and disable time	En	–	10	–	10	–	10	ns
		Dis	–	40	–	40	–	40	ns
D_R	Data rate(1)		–	6.4	–	4.5	–	3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Table 11. AC characteristics - test conditions: V_L = 2.5 - 2.7 V (device driven by totem pole driver)

Symbol	Parameter		V_{CC} = 2.7 - 3.6 V		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}		–	3.8	–	2.8	ns
t_{FVCC}	Fall time I/O_{VCC}		–	14.8	–	19.1	ns
t_{RVL}	Rise time I/O_{VL}		–	3.3	–	3.2	ns
t_{FVL}	Fall time I/O_{VL}		–	9.8	–	10.0	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	–	3.2	–	2.8	ns
		t_{PHL}	–	8.2	–	11.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	–	2.6	–	2.0	ns
		t_{PHL}	–	5.3	–	5.9	ns
t_{PZL} t_{PLZ}	Output enable and disable time	En	–	6	–	6	ns
		Dis	–	40	–	40	ns
D_R	Data rate(1)		–	9	–	6.8	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Table 12. AC characteristics - test conditions: V_L = 2.7 - 3.6 V (device driven by totem pole driver)

Symbol	Parameter		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}		–	2.9	ns
t_{FVCC}	Fall time I/O_{VCC}		–	17.2	ns
t_{RVL}	Rise time I/O_{VL}		–	3.0	ns
t_{FVL}	Fall time I/O_{VL}		–	9.7	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	–	2.7	ns
		t_{PHL}	–	10.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	–	1.9	ns
		t_{PHL}	–	4.8	ns
t_{PZL} t_{PLZ}	Output enable and disable time	En	–	6	ns
		Dis	–	40	ns
D_R	Data rate(1)		–	7.2	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Figure 4. Test circuit

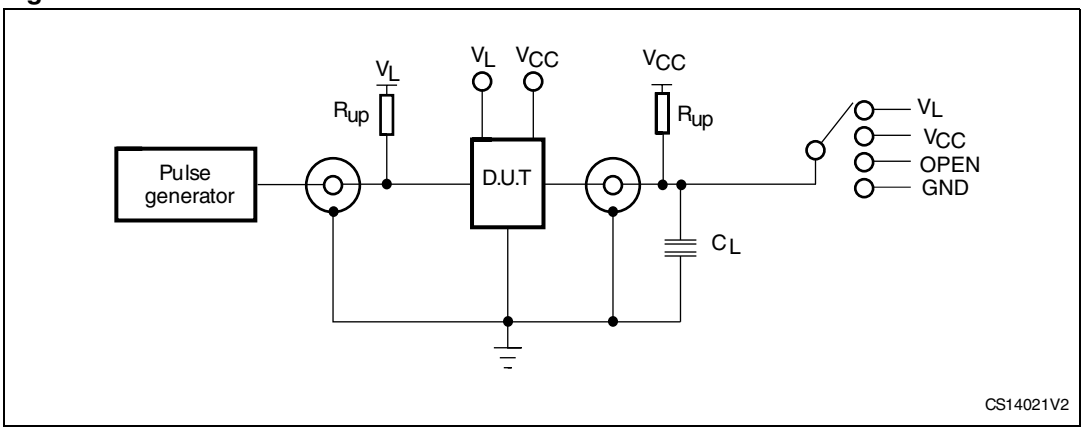


Table 13. Test circuit switches

Test	Switch		
	Driving I/O_{VL}	Driving I/O_{VCC}	Open drain driving
t_{PLH}, t_{PHL}	Open	Open	Open

7 Waveforms

Table 14. Waveform symbol value

Symbol	Driving I/O_{VL}		Driving I/O_{VCC}	
	1.8 V ≤ V_L ≤ V_{CC} ≤ 2.5 V	**3.3 V ≤ V_L ≤ V_{CC} ≤ 5.0 V**	**1.8 V ≤ V_L ≤ V_{CC} ≤ 2.5 V**	**3.3V ≤ V_L ≤ V_{CC} ≤ 5.0 V**
V_{IH}	V_L	V_L	V_{CC}	V_{CC}
V_{IM}	50% V_L	50% V_L	50% V_{CC}	50% V_{CC}
V_{OM}	50% V_{CC}	50% V_{CC}	50% V_L	50% V_L

Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)

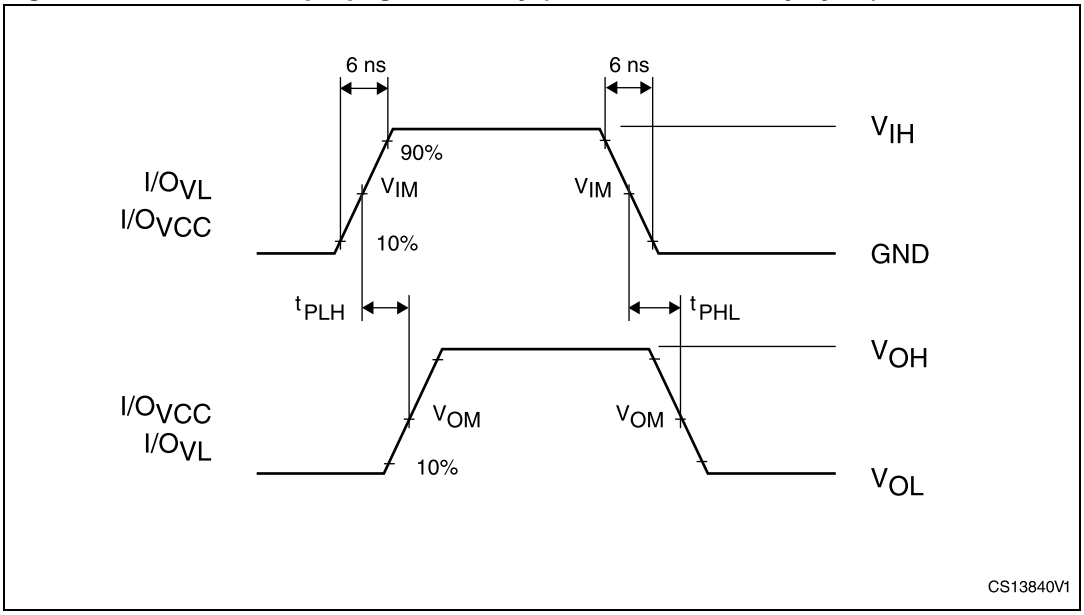
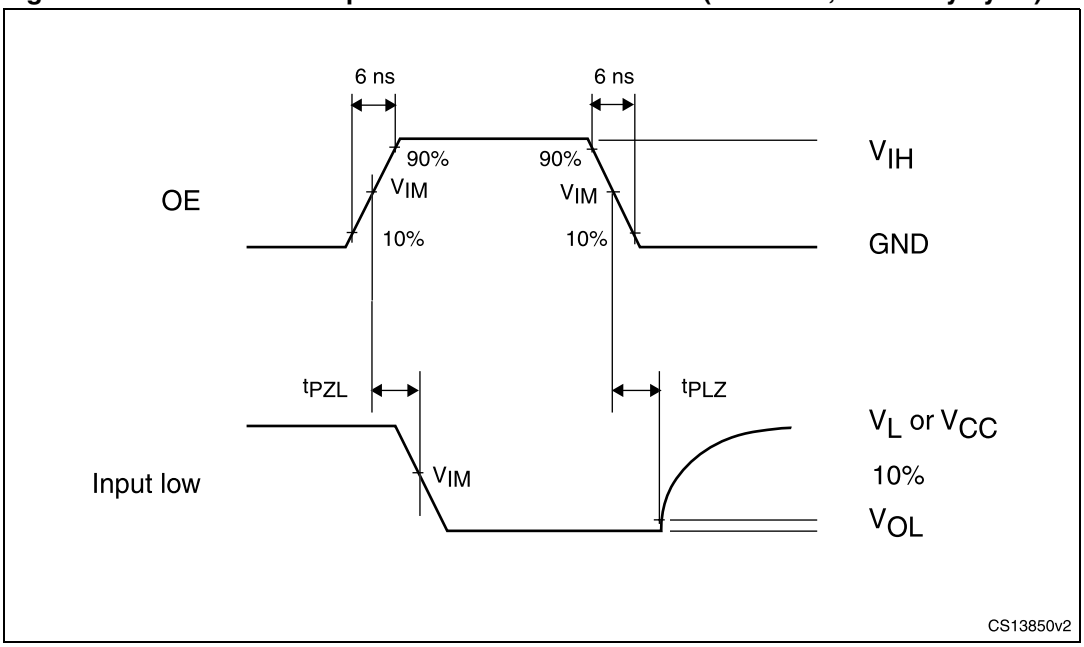


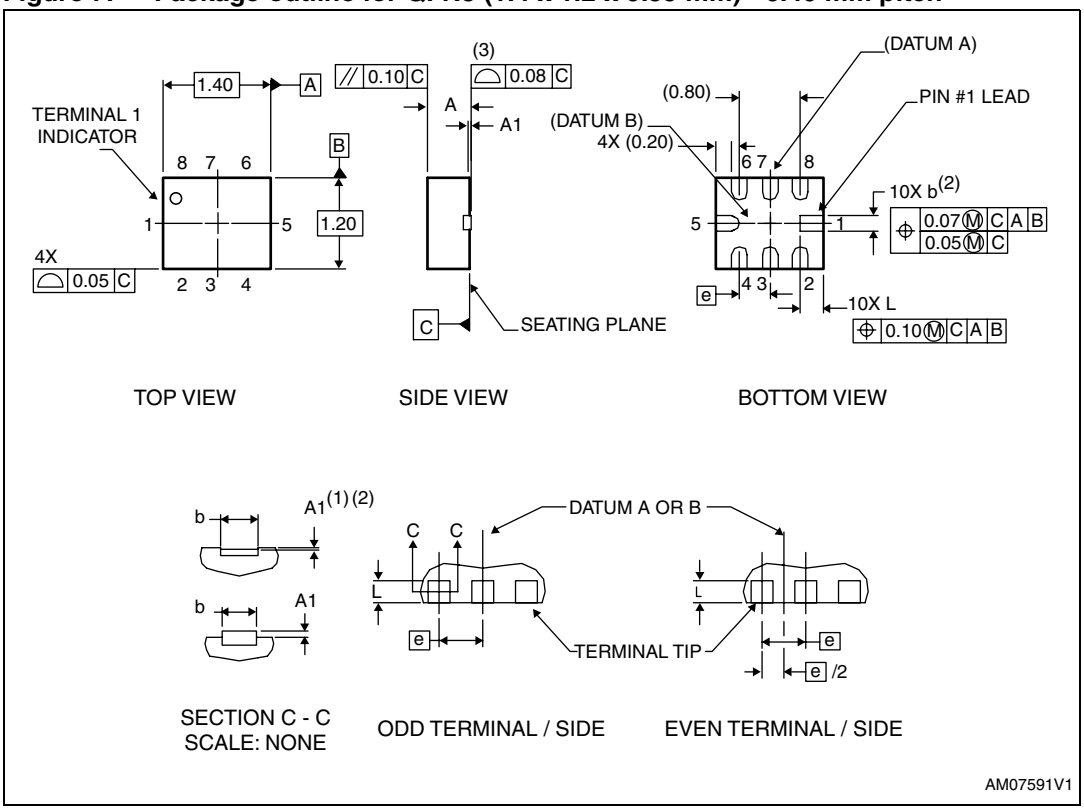
Figure 6. Waveform - output enable and disable time (f = 1 MHz; 50% duty cycle)



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 7. Package outline for QFN8 (1.4 x 1.2 x 0.55 mm) - 0.40 mm pitch



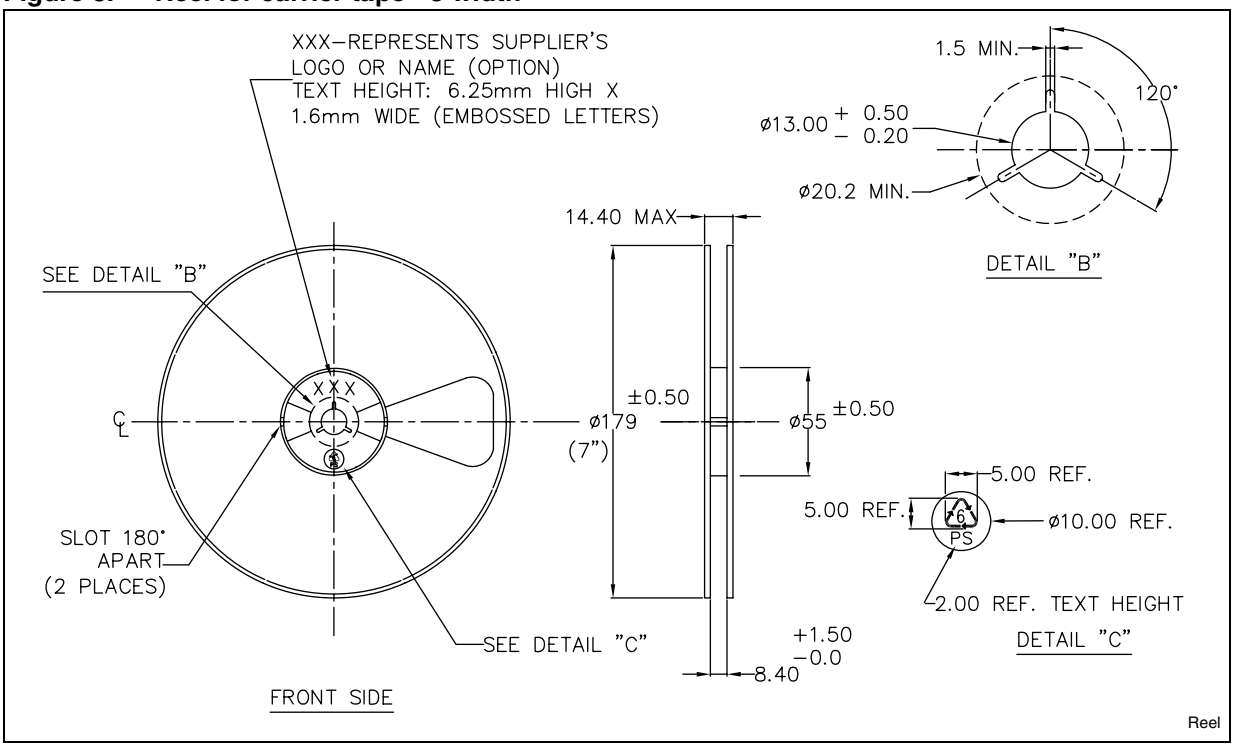
1. Dimension b applies to the metallized terminal and is measured between 0.10 and 0.20 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, dimension b should not be measured in that radius area.
2. Applied only for terminals.
3. Bilateral coplanarity zone applies to the exposed heatsink slug as well as the terminals.
4. Dimensions and tolerancing conform to ASME Y14.5M - 1994.

Table 15. Mechanical data for QFN8 (1.4 x 1.2 x 0.55 mm) - 0.40 mm pitch

Symbol	Dimensions			Note
	Millimeters			
	Min.	Nom.	Max.	
A	0.50	0.55	0.60	
A1	0.00	-	0.05	
b	0.15	0.20	0.25	(1)
B	0	-	12°	(2)
e	0.40 BSC			
N	8			(3)
L	0.25	0.30	0.35	

1. Dimension b applies to the metallized terminal and is measured between 0.10 and 0.20 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, dimension b should not be measured in that radius area.
2. All dimensions are in millimeters, B is in degrees.
3. N is the total number of terminals.

Figure 8. Reel for carrier tape - 8 width



9 Revision history

Table 16. Document revision history

Date	Revision	Changes
25-Jun-2012	1	Initial release.

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